Preliminary Data Sheet

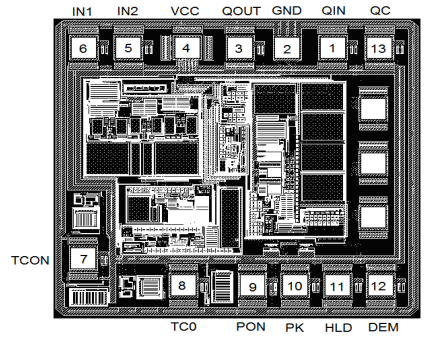
CE 6005

RC Receiver IC

RF Technology Specialist

CE 6005

Single and dual band receiver IC



芯片面积： 1.34mm*1.32mm
PAD窗口： 85um*85um

1 Short Description

The CE 6005 is a BiCMOS integrated straight through receiver with build in very high sensitivity for the time signal transmitted from WWVB, DCF77, JJY, MSF and HBG. The receiver is prepared for single-and dual band (by using additional capacitor matching pin) reception. Integrated functions as stand by mode, complementary output stages and hold mode function offer features for universal applications. The power down mode increases the battery lifetime significantly and makes the device ideal for all kinds of radio controlled time pieces.

2 Features

- Low power consumption (<100µA)
- Very high sensitivity (0.4µV)
- Dedicated input for external crystal capacitance matching for dual band application
- High selectivity by using crystal filter
- Power down mode
- Only a few external components necessary
- AGC hold mode
- Wide frequency range (40 ... 120 kHz)
- Low power applications (1.2 .. 5.0 V)
- Improved noise resistance
- Integrated AGC adaptation

Benefits

- Dual band application
- Existing software can be used
- Extended battery operating time

Block Diagram

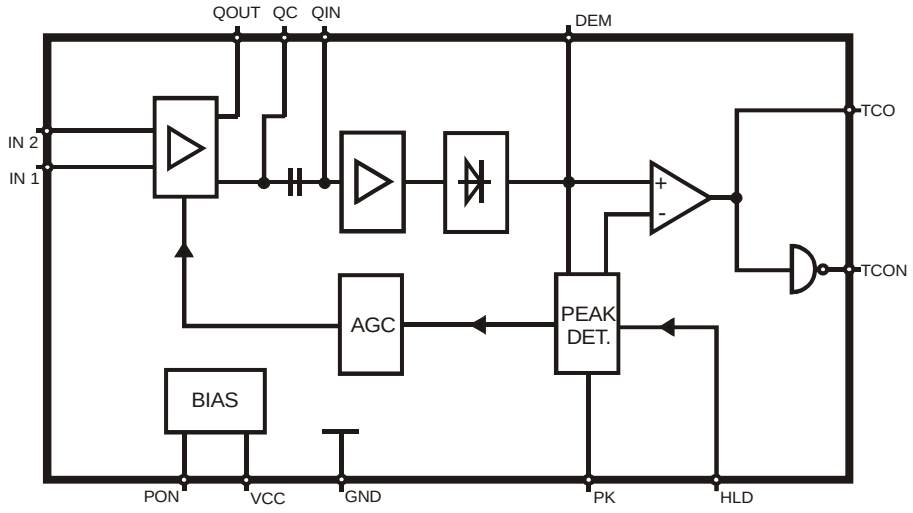


Figure 1. Block diagram

3 Ordering Information

Extended Type Number	Package	Remarks
CE6005-DDT	no	die in trays
CE6005-TCSH	yes	SSO16
CE6005-TCQH	Yes	SSO16 Taped and reeled
*The packaged version of CE6005 complies with lead free JEDEC standard J-STD 020B.		

4 Absolute Maximum Ratings

Parameters	Symbol	Value	Unit
Supply voltage	VCC	5.5	V
Ambient temperature range	T_{amb}	-40 to +85	°C
Storage temperature range	R_{stg}	-55 to +150	°C
Junction temperature	T_j	125	°C
Electrostatic handling (MIL Standard 883 D HBM)	+/- V_{ESD}	+/-4000	V
Electrostatic handling (MIL MM)	+/- V_{ESD}	+/-400	V

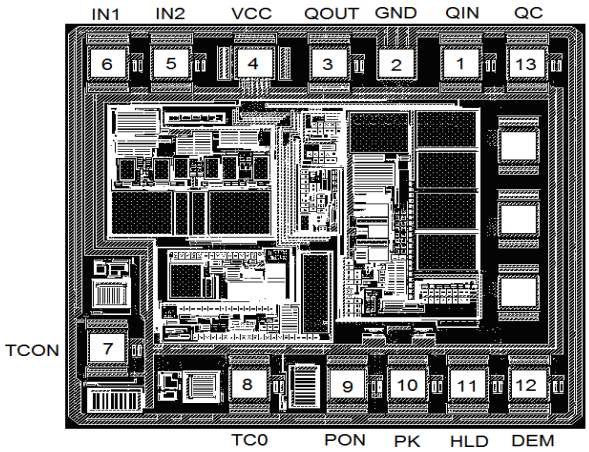
5 PAD Coordinates

The CE6005 is available as die for "chi
DIE size: 1,34mm x 1,32mm
PAD size: 100 x 100 µm (contact window 84µm / 84µm)
Thickness: 300µm±10µm

Symbol	Function	x-axis (µm)	y-axis (µm)	Pad # (dice)	Pin # (SSO16*)
QIN	Crystal Input	118,5	1138,2	1	2
GND	Ground	118,5	969,6	2	3
QOUT	Crystal output	118,5	803,3	3	4
VCC	Supply voltage	118,5	464,8	4	5
IN2	Antenna input 2	118,5	304,8	5	6
IN1	Antenna input 1	118,5	99,6	6	7
TCON	Negative signal output	1039,5	87,6	7	10
TCO	Positive signal output	1167,8	471,3	8	11
PON	Power ON input	1167,8	738,4	9	12
PK	Capacity for AGC	1167,8	924,3	10	13
HLD	AGC hold	1167,8	1141,5	11	14
DEM	Demodulator output	1167,8	1326,4	12	15
QC	Crystal matching Cap	118,5	1319,1	13	1

Coordinate requirements should be achieved

6- Pad Layout



芯片面积： 1.34mm*1.32mm
PAD窗口： 85um*85um

Pin Layout SSO16

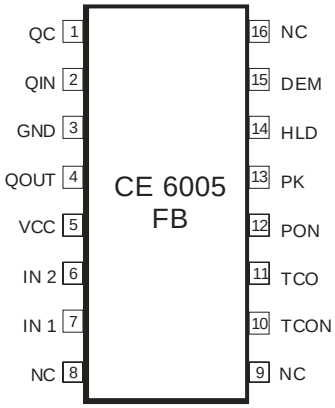


Figure 3. Pin layout SSO16

PIN Description

IN1, IN2

A ferrite antenna is connected between IN 1 and IN 2. For high sensitivity, the Q factor of the antenna circuit should be as high as possible. Please note that a high Q factor requires temperature compensation of the resonant frequency in most cases. We recommend a Q factor between 40 and 150, depending on the application. An optimal signal-to-noise ratio will be achieved by a resonator resistance of 40 kΩ to 100 kΩ.

QOUT, QIN , QC

In order to achieve a high selectivity, a crystal is connected between the Pins QOUT and QIN. It is used with the serial resonant frequency according to the time-code transmitter and acts as a serial resonator. Up to 2 crystals can be connected parallel between QOUT and QIN. For one crystal, the given parallel capacitor of the filter crystal (about 1.4 pF) is internally compensated so that the bandwidth of the filter is about 10 Hz. For two crystals, an additional external capacitor with the value of about 1.4 pF has to be connected parallel between QC and QIN. The impedance of QIN is high. Parasitic loads have to be avoided.

DEM

Demodulator output. To ensure the function, an external capacitor has to be connected at this output.

HLD

AGC hold mode: HLD high ($V_{HLD} = V_{CC}$) sets normal function, HLD low ($V_{HLD} = 0$) holds for a short time the AGC voltage. This can be used to prevent the AGC from peak voltages, created by e.g. a stepper motor

PK

Peak detector output. An external capacitor has to be connected to ensure the function of the AGC regulation. The value of the capacitance influences the AGC regulation time.

NOTE: To realize a good regulation timing of the demodulator and the peak detector the value of the capacitors at DEM and PK have to be changed for the different protocols.

VCC, GND
V_{CC} and GND are the supply voltage inputs. The positive supplies have to be connected externally, and also the ground pins.
To power down the circuitry it is recommended to use the PON input and not to switch the power supply. Switching the power supply results in a long power up waiting time.

PON
If PON is connected to GND, the receiver will be activated. The setup time is typically 0.5 sec after applying GND to this pin. If PON is connected to VCC, the receiver will switch to Power Down mode.

TCO, TCON
The serial signal of the time-code transmitter can be directly decoded by a micro controller. Details about the time-code format of several transmitters are described separately. If TCO is connected, TCON must be open or counterwise.

7 Design Hints for the Ferrite Antenna

7.1 Dimensioning of antenna circuit for different clock/watch applications

The bar antenna is a very critical device of the complete clock receiver. Observing some basic RF design rules helps to avoid possible problems. The IC requires a resonant resistance of 40 kΩ to 100 kΩ. This can be achieved by a variation of the L/C-relation in the antenna circuit. In order to achieve this resonant resistance, we recommend to use antenna capacitors of a value between 2.2nF and 6.8nF. The optimum value of the capacitor has to be specified respecting the concrete application needs and different boundary conditions(ferrite material, type of antenna wire, available space for antenna coil).It is not easy to measure such high resistances in the RF region. A more convenient way is to distinguish between the different bandwidths of the antenna circuit and to calculate the resonant resistance afterwards.
Thus, the first step in designing the antenna circuit is to measure the bandwidth. Figure 12 shows an example for the test circuit. The RF signal is coupled into the bar antenna by inductive means, e.g., a wire loop. It can be measured by a simple oscilloscope using the 10:1 probe. The input capacitance of the probe, typically about 10 pF, should be taken into consideration. By varying the frequency of the time signal generator, the resonant frequency can be determined.

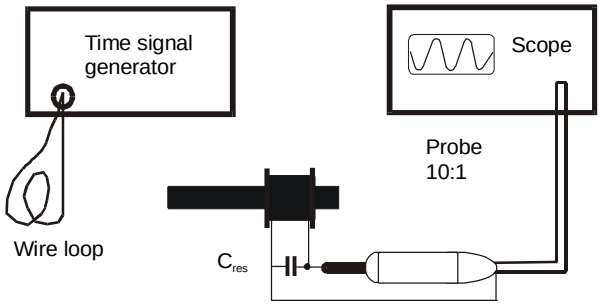


Figure 12.

At the point where the voltage of the RF signal at the probe drops by 3 dB, the two frequencies can then be measured. The difference between these two frequencies is called the bandwidth BW_A of the antenna circuit. As the value of the capacitor C_{res} in the antenna circuit is known, it is easy to compute the resonant resistance according to the following formula:

$$R_{res}=\frac{1}{2 \times \pi \times BW_A \times C_{res}}$$

Where
R_{res} is the resonant resistance,
BW_A is the measured bandwidth

C_{res} is the value of the capacitor in the antenna circuit (Farad).
If high inductance values and low capacitor values are used, the additional parasitic capacitance of the coil must be considered. The Q value of the capacitor should be no problem if a high Q type is used. The Q value of the coil differs more or less from the DC resistance of the wire. Skin effects can be observed but do not dominate.
Therefore, it should not be a problem to achieve the recommended values of the resonant resistance. The use of thicker wire increases the Q value and accordingly reduces bandwidth. This is advantageous in order to improve reception in noisy areas. On the other hand temperature compensation of the resonant frequency might become a problem if the bandwidth of the antenna circuit is low compared to the temperature variation of the resonant frequency. Of course, the Q value can also be reduced by a parallel resistor.

Temperature compensation of the resonant frequency is a must if the clock is used at different temperatures. Please ask your supplier of bar antenna material and of capacitors for specified values of the temperature coefficient.

Furthermore, some critical parasitics have to be considered. These are shortened loops (e.g., in the ground line of the PCB board) close to the antenna and undesired loops in the antenna circuit. Shortened loops decrease the Q value of the circuit. They have the same effect like conducting plates close to the antenna. To avoid undesired loops in the antenna circuit, it is recommended to mount the capacitor C_{res} as close as possible to the antenna coil or to use a twisted wire for the antenna-coil connection. This twisted line is also necessary to reduce feedback of noise from the microprocessor to the IC input. Long connection lines must be shielded.

A final adjustment of the time-code receiver can be carried out by pushing the coil along the bar antenna.

7.2 Dimensioning of capacitor C_{DEM}

The value of 22nF for capacitor C_{DEM} as shown in chapter 9 and 10 represents the minimum value for frequency of 77.5 kHz. For lower frequencies (40kHz, 60kHz) a minimum value of C_{DEM}=47nF should be used. For a better damping of noise and other interference it is recommended to double the values of C_{DEM},. That means C_{DEM} = 47nF for 77.5kHz and C_{DEM} = 100nF for 40kHz and 60kHz. This optimization has to be done according to each application.

8 Electrical Characteristics

V_{CC} = 3V, input signal frequency 77.5 kHz +/- 5 Hz; carrier voltage 100% reduction to 25% for t_{MOD} = 200ms; t_{amb} = 25°C, max./min. limits are at +25...C ambient temperature, unless otherwise specified.

Parameter	Test condition / Pin	Symbol	Min.	Typ.	Max.	Unit
Supply voltage range	Pad/Pin V_{CC}	V_{CC}	1.2		5.5	V
Supply current	Pad/Pin V_{CC}	I_{CC}		<90	100	µA
Set-up time after V_{CC} ON	V_{CC} = 3V	t		1.5		s
Reception frequency range		F_{in}	40		120	kHz
Minimum input voltage	Pad/Pin IN1, IN2	V_{in}		0.4	0.6	µV
Maximum input voltage	Pad/Pin IN1, IN2	V_{in}	30	50		mV
Input amplifier max. gain (V_{PK} = 0.2V)		V_{U1}		47		dB
Input amplifier min. gain (V_{PK} = 0.8V)		V_{U2}		-40		dB
Pins TCO, TCON Output low Output high	 Iol = 10µA Ioh = -10µA		 0.9 x Vcc		 0.1 x V_{CC}	 V V
Power-ON control; PON	**Pad/Pin PON**					
Input level Input leakage current	Low level High level $0<V_i<V_{cc}$		 0.85 V_{cc} -0.1		0.15 V_{cc} 0.1	V V µA
Quiescent current receiver OFF	$V_{PON}=V_{CC}$, Pad/Pin V_{CC}	I_{CC0}		0.03	0.05	µA
Set-up time after PON		t		0.5	2	s
AGC hold mode; HLD	**Pad/Pin HLD**					
Input level Input leakage current	Low level High level $0<V_i<V_{cc}$		 0.85 V_{cc} -0.1		0.15 V_{cc} 0.1	V V µA
AC characteristics						
Output pulse width for TCO and TCON	Modulation according DCF, 200 ms pulse	t_{WO200}	170	195	230	ms
Output pulse width for TCO and TCON	Modulation according DCF, 100 ms pulse	t_{WO100}	70	95	130	ms

9 Test Circuitry for single frequency reception

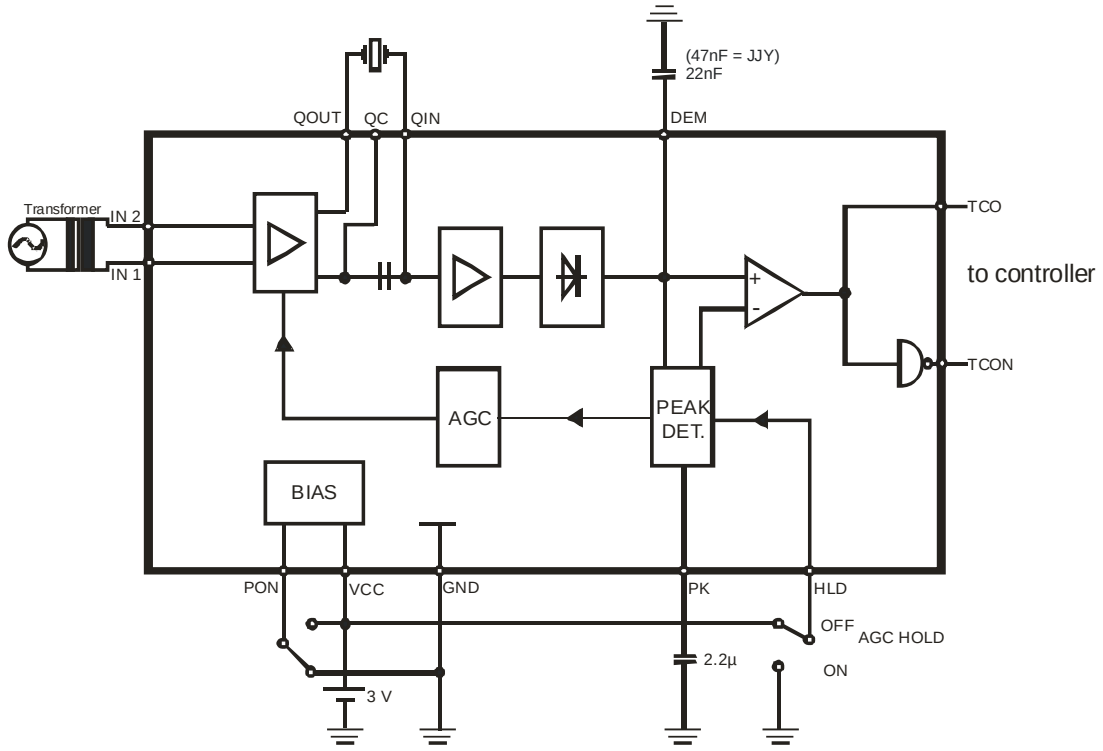


Figure 12. Test circuit

10 Test Circuitry for dual frequency reception

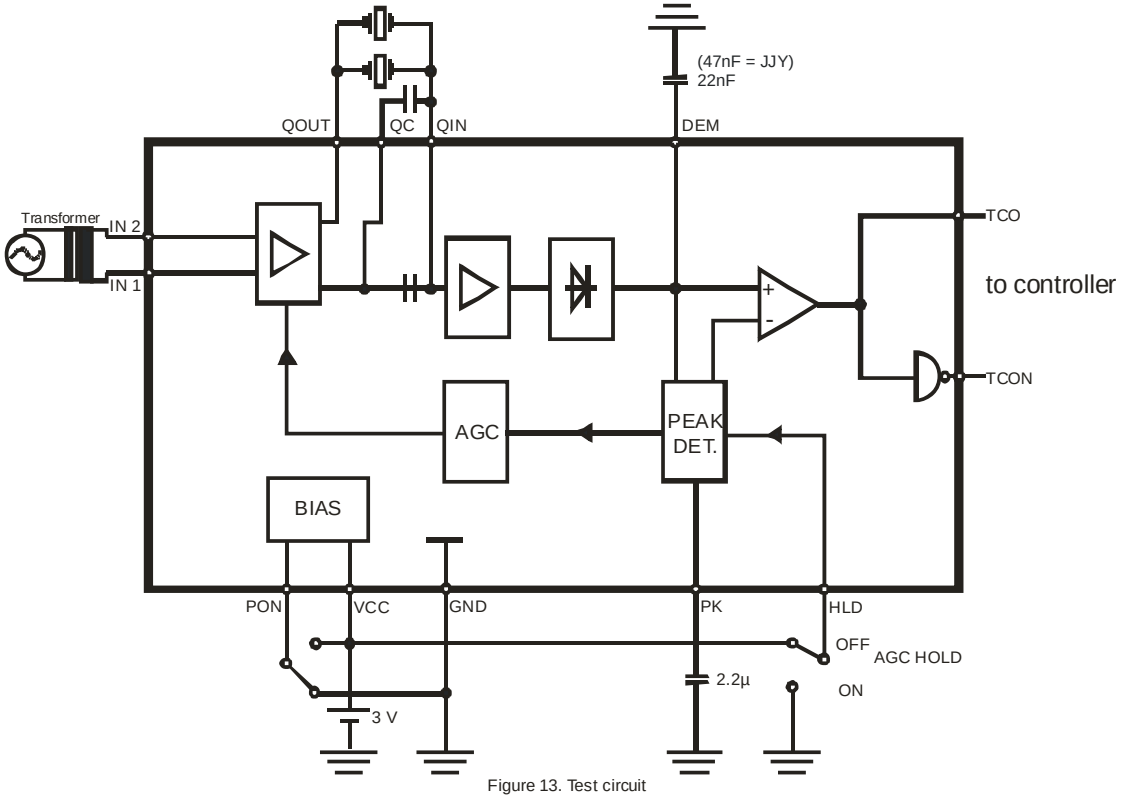


Figure 13. Test circuit

11 Information on the German Transmitter

(Customer is responsible to verify this information)

Station:	DCF 77	Location:	Mainflingen/Germany
Frequency:	77.5 kHz	Geographical coordinates:	50° 01'N, 09° 00'E
Transmitting power:	50 kW	Time of transmission:	permanent

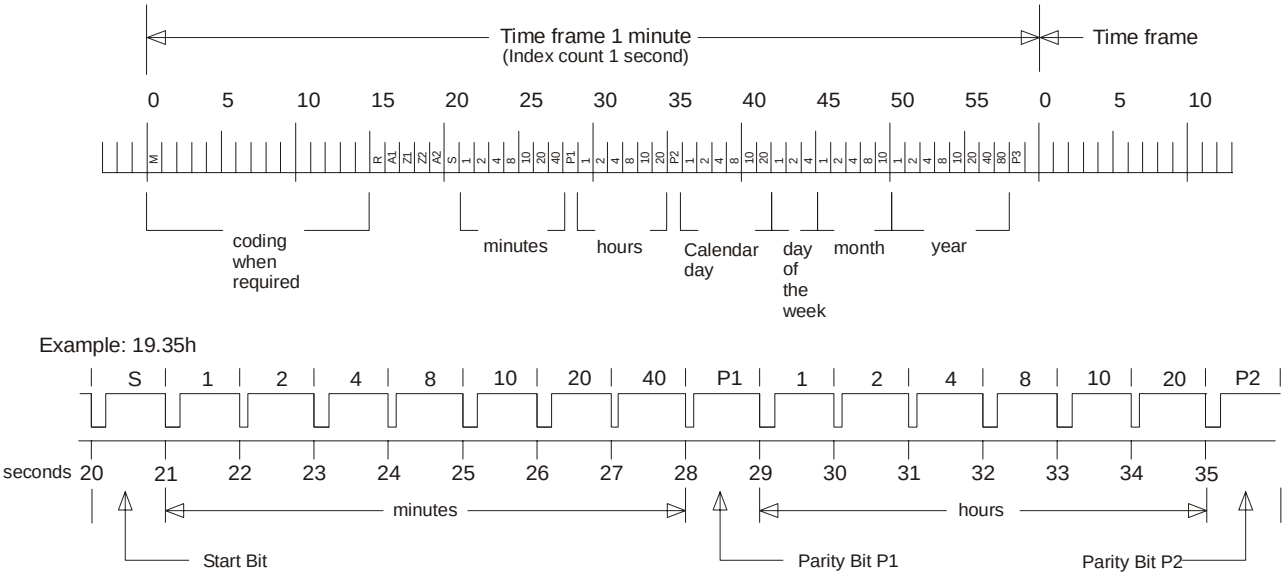


Figure 15.

M =	Minute marker (100ms)	Z2 =	DST (wintertime = 200ms, otherwise 100ms)
R =	Second marker (200ms = transmission by reserve antenna)	A2 =	Announcement of leap second
A1 =	Announcement of change-over to summer-time or vice versa)	S =	Startbit of time code information
Z1 =	DST (summertime = 200ms, otherwise 100ms)	P1-P3 =	Parity check bits

Modulation

The carrier amplitude is reduced to 25% at the beginning of each second for a period of 100 ms (binary zero) or 200 ms (binary one), except the 59th second.

Time-Code Format (based on Information of Deutsche Bundespost)

The time-code format consists of 1-minute time frames. There is no modulation at the beginning of the 59th second to indicate the switch over to the next 1-minute time frame. A time frame contains BCD-coded information of minutes, hours, calendar day, day of the week, month and year between the 20th second and 58th second of the time frame, including the start bit S (200 ms) and parity bits P1, P2 and P3. Furthermore, there are 5 additional bits R (transmission by reserve antenna), A1 (announcement of change-over to summer time), Z1 (during summer time 200 ms, otherwise 100 ms), Z2 (during winter time 200 ms, otherwise 100 ms) and A2 (announcement of leap second) transmitted between the 15th second and 19th second of the time frame.

12 Information on the Swiss Transmitter

(Customer is responsible to verify this information)

Station:	HBG	Location:	Prangins/Switzerland
Frequency:	75 kHz	Geographical coordinates:	46° 24'N, 06° 15'E
Transmitting power:	20 kW	Time of transmission:	permanent

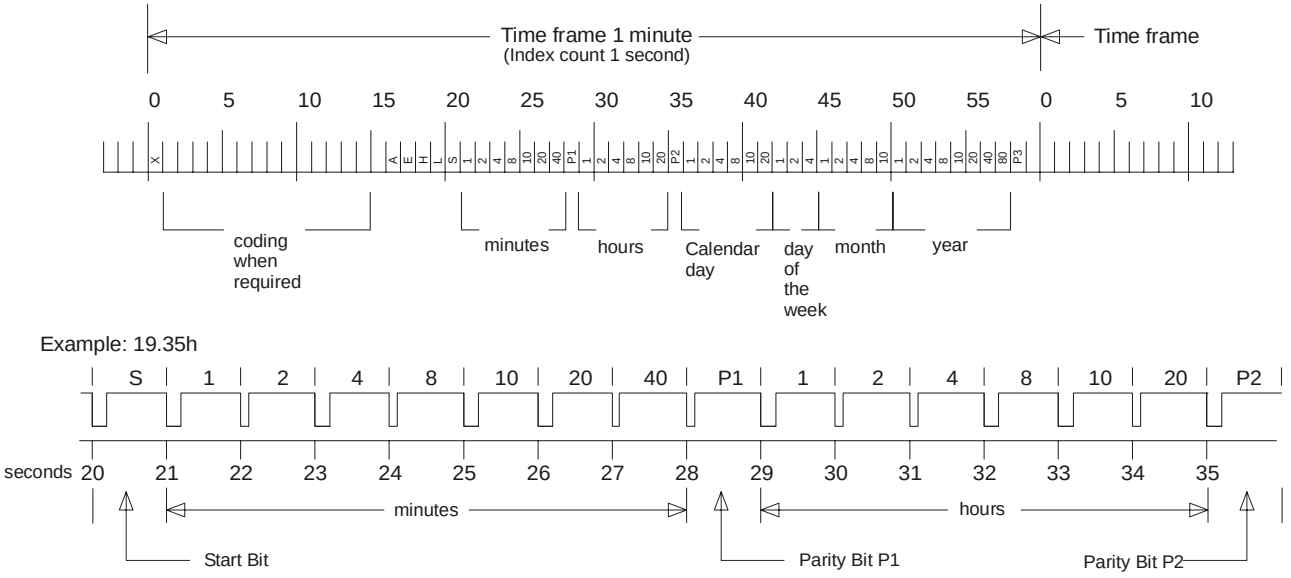


Figure 15.

X =	Minute marker	L=	Announcement of leap second
A =	Announcement of change over to summer time or vice-versa	S=	Startbit of timecode information
E=	DST (summertime = 200ms, otherwise 100ms)	P1-P3=	Partiy check bits
H=	DST (wintertime = 200ms, otherwise 100ms)		

Modulation

The carrier amplitude is reduced to 25% at the beginning of each second for a period of 100 ms (binary zero) or 200 ms (binary one), except the 59th second.

Time-Code Format (based on Information of Bundesamt für Metrologie und Akkreditierung (METAS))

The time-code format consists of 1-minute time frames. There is no modulation at the beginning of the 59th second to indicate the switch over to the next 1-minute time frame. A time frame contains BCD-coded information of minutes, hours, calendar day, day of the week, month and year between the 20th second and 58th second of the time frame, including the start bit S (200 ms) and parity bits P1, P2 and P3. Furthermore, there are 5 additional bits R (transmission by reserve antenna), A (announcement of change-over to summer time), E (during summer time 200 ms, otherwise 100 ms), H (during winter time 200 ms, otherwise 100 ms) and L (announcement of leap second) transmitted between the 15th second and 19th second of the time frame.

13 Information on the British Transmitter

(Customer is responsible to verify this information)

Station:	MSF	Location:	Rugby
Frequency:	60 kHz	Geographical coordinates:	52° 22'N, 01° 11'W
Transmitting power:	50 kW	Time of transmission:	permanent, except for quarterly and annual outages

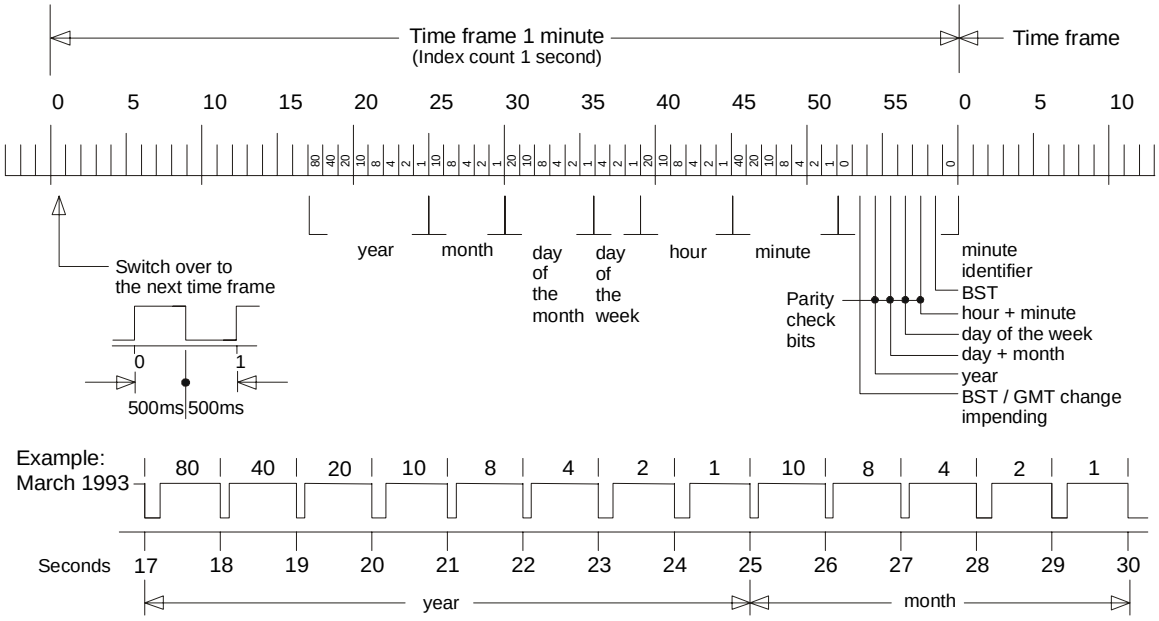


Figure 16.

Modulation

The carrier amplitude is switched off at the beginning of each second for a period of 100 ms (binary zero) or 200 ms (binary one).

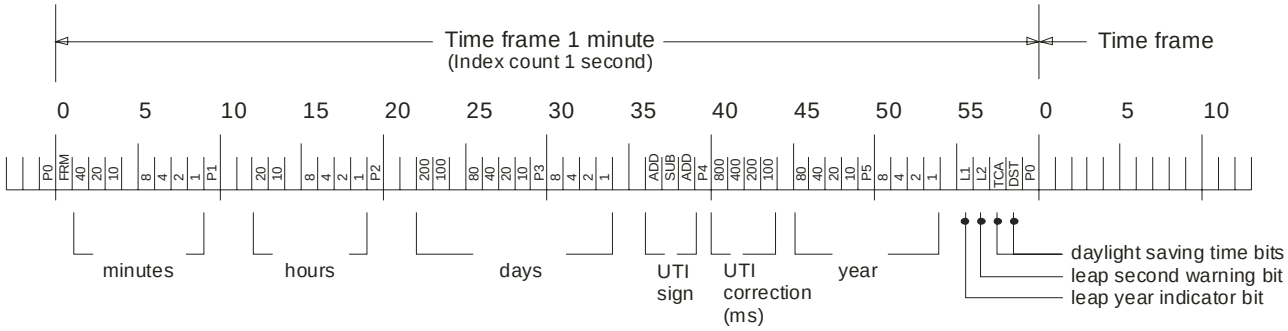
Time-Code Format

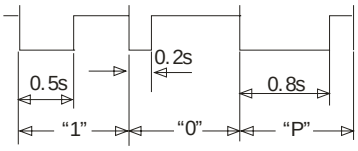
The time-code format consists of 1-minute time frames. A time frame contains BCD coded information of year, month, calendar day, day of the week, hours and minutes. At the switch-over to the next time frame, the carrier amplitude is reduced for a period of 500 ms.
The presence of the fast code during the first 500 ms at the beginning of the minute is not guaranteed. The transmission rate is 100 bit/s and the code contains information of hour, minute, day and month.

14 Information on the US Transmitter

(Customer is responsible to verify this information)

Station:	WWVB	Location:	Fort Collins/Colorado
Frequency:	60 kHz	Geographical coordinates:	40° 40'N, 105° 03' W
Transmitting power:	50 kW	Time of transmission:	permanent





FRM = Frame Marker

L1 = Leap year indicator
"1" = non leap year
"0" = leap year
The bit is set to 1 during each leap year after January 1 but before February 29. It is set back to 0 on January 1 of the year following the leap year.

L2 = Leap second warning bit
The bit is set to 1 near the start of the month in which a leap second is added. It is set to 0 immediately after the leap second insertion.

TCA = Time change announcement

DST = Daylight savings time bit

P0 - P5 = Position marker

Modulation

The carrier amplitude is reduced by 10 dB at the beginning of each second and is restored within 500 ms (binary one) or within 200 ms (binary zero) or within 800 ms (position-identifier marker or frame reference marker).

Time-Code Format

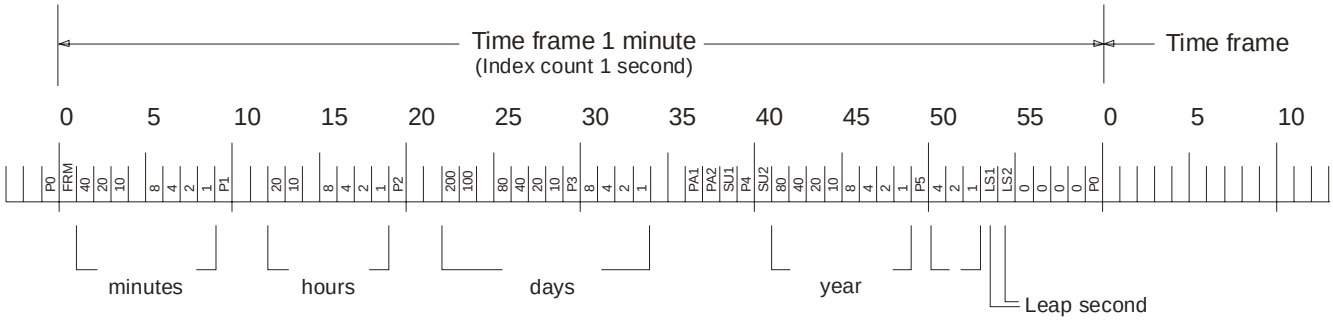
The time-code format consists of 1-minute time frames. A time frame contains BCD-coded information of minutes, hours, days and year. In addition, there are 6 position-identifier markers (P0 thru P5) and 1 frame-reference marker with reduced carrier amplitude of 800 ms duration

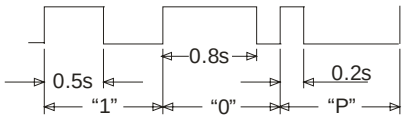
15 Information on the Japanese Transmitter

(Customer is responsible to verify this information)

Station:	Ohtakadoya-yama	Location:	Miyakoji Vil.,Fukushima Pref.
Frequency:	40 kHz	Geographical coordinates:	37° 22'N, 140° 51'E
Transmitting power:	50 kW	Time of transmission:	permanent

Station:	Hagane-yama	Location:	Fuji Vil., Saga Pref.
Frequency:	60 kHz	Geographical coordinates:	33° 28'N, 130° 11'E
Transmitting power:	50 kW	Time of transmission:	permanent





0.5 second: Binary one
0.8 second: Binary zero
0.2 second: Position identifier markers P0...P5

FRM = Frame marker
LS1 = Leap second
LS2 = Leap second
P0-P5 = Position identifier markers
Pa1+Pa2 = Parity bits

Modulation

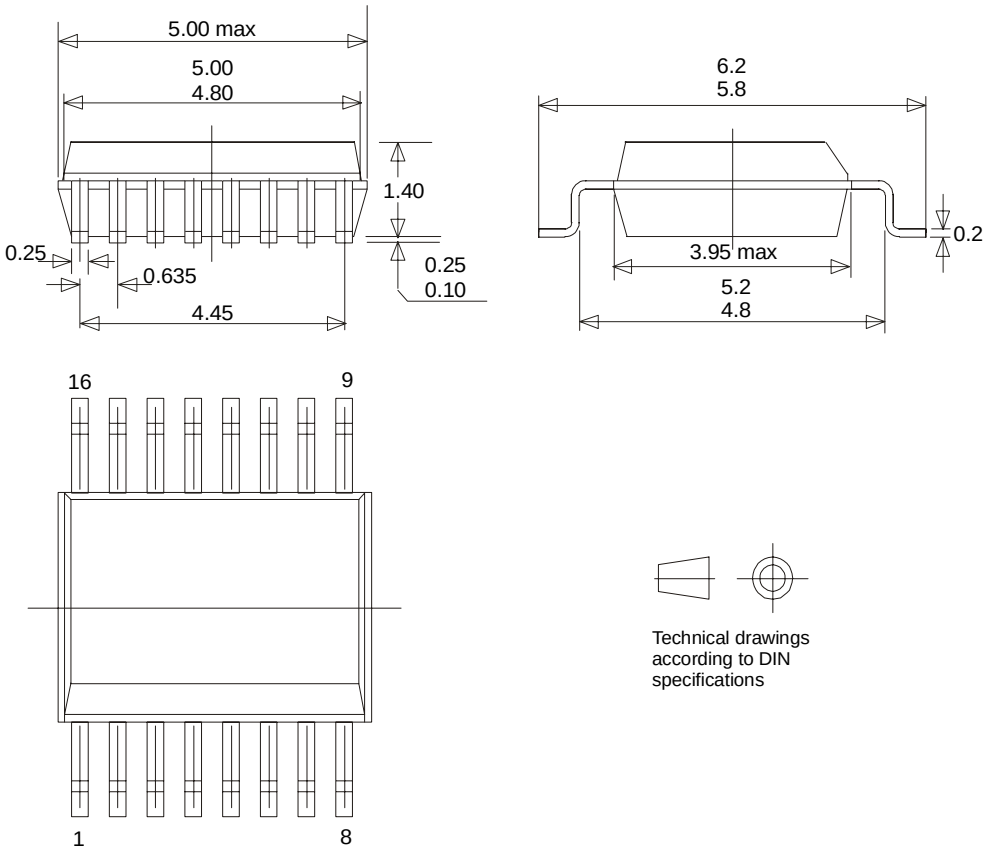
The carrier amplitude is 100% at the beginning of each second and is switched to 10% after 500 ms (binary one) or after 800 ms (binary zero) or after 200 ms for Position-identifier marker (P0...P5) and frame reference marker.

Time-Code Format

The time-code format consists of 1-minute time frames. A time frame contains BCD-coded information of minutes, hours, days, weeks and year. In addition, there are 6 position-identifier markers (P0 through P5) with reduced carrier amplitude of 800 ms duration.

16 Package information

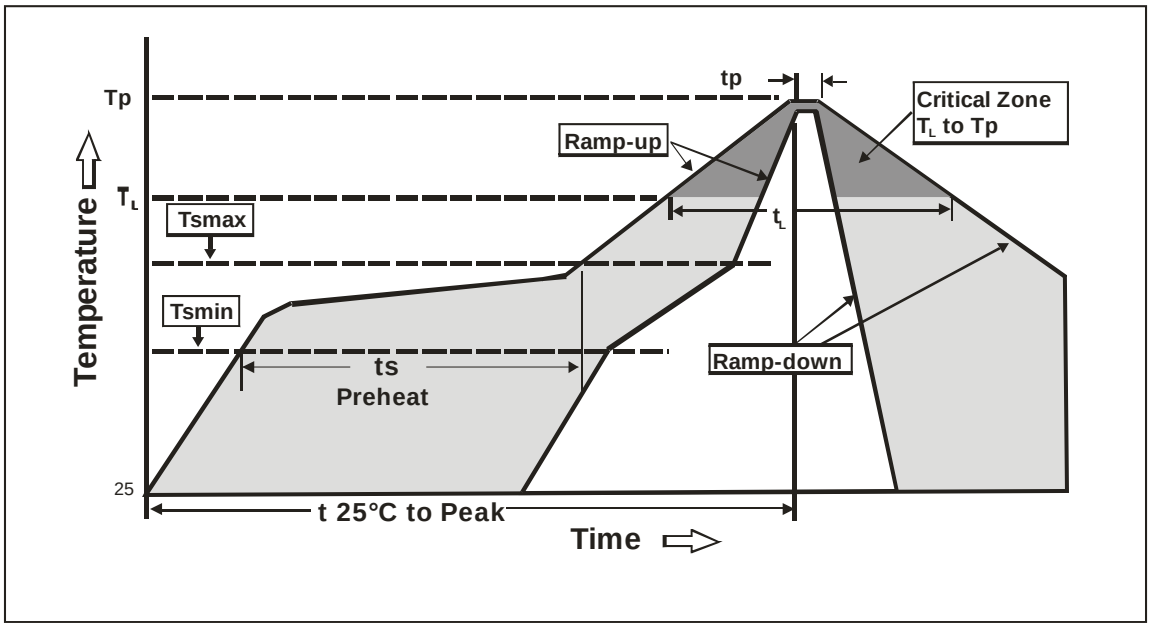
Package SSO16
Dimensions in mm



Technical drawings according to DIN specifications

Recommended Infrared/Convection Solder Reflow Profile (SMD packages)

Profile Feature	Pb-free assembly
Average ramp-up rate (T_L to T_P)	3°C/second max.
Preheat - Temperature Min (T_{Smin}) - Temperature Max (T_{Smax}) - Time (min to max) (ts)	 150°C 200°C 60-180 seconds
T_{Smax} to T_L - Ramp-up rate	 3°C/second max.
Time maintained above: - Temperature (T_L) - Time (t_L)	 217°C 60-150 seconds
Peak Temperature (T_P)	260 +0/-5°C
Time within 5°C of actual Peak Temperature (t_P)	20-40 sec.
Ramp-down rate	6°C/second max.
Time 25°C to Peak Temperature	8 minutes max.



Recommended Wave Soldering (Through hole packages)

Condition	Symbol	Value	Unit
Maximum lead temperature (5s)	T_D	260	°C